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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
NGUYEN, MIKE	
ART UNIT	**PAPER NUMBER**
2182	

DATE MAILED: 09/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/605,325	MOORE, MICHAEL T.	
	Examiner	Art Unit	
	Mike Nguyen	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 May 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22 and 24* is/are rejected.

7)☒ Claim(s) *23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Notices & Remarks

1. Applicant's amendment file on 05/10/2004 in response to Examiner's Office Action has been reviewed but they are not deemed to be persuasive.

2. Claims 1-24 are pending for the examination.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 21-22 and 24 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The specification is silent regarding "an interface configured to couple said programmable logic device with said memory circuit, wherein said programmable logic device is configured by said memory circuit during bootup", "an interface configured to couple said processor with said memory circuit, wherein said processor is configured to perform one or more of (i) programming said memory circuit, (ii) reading said memory circuit, (iii) verifying said memory circuit and (iv) erasing said memory circuit", "a first interface configured to couple said programmable logic device with said memory circuit, wherein said programmable logic device is configured by said memory circuit during bootup", and "a second interface configured to couple said processor with said memory circuit".

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-2, 5-6,10-15, 17-18, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tang et al. (U.S. Pat. No. 6,389,321 B2) in view of Lien et al. (U.S. Pat. No. 6,446,242 B1).

6. As to claim 1, Tang teaches an apparatus (see fig. 5) comprising:

a wireless transceiver coupled to a programmable logic circuit (see fig. 5 elements 501, 402), wherein said programmable logic circuit comprises a processor, and memory circuit in a single circuit (IC) package (see fig. 8 elements 803, 804, 801, 807 and col. 3 line 63 to col. 4 line 11).

Although the apparatus disclosed by Tang shows substantial features of the claimed invention (discussed above), it fails to explicitly teach: a programmable logic device. Lien; however, teaches said programmable logic circuit comprises a programmable logic device (see fig. 1 elements 20, 22 and col. 3 lines 29-45). Given the teaching of Lien, a person having ordinary skill in the art would have readily recognized the desirability and advantages of modifying Tang by employing the well-known or conventional feature of the apparatus, such as taught by Lien, in order to provide integrating multiple components into a single integrated circuit package.

7. As to claim 2, Tang teaches the apparatus according to claim 1, wherein said single integrated circuit package contains one or more integrated circuit dies (see fig. 8 elements 801-807 and col. 3 lines 63-67).

8. As per claims 5 and 6, Tang teaches the apparatus wherein said wireless transceiver communicates using either electromagnetic or ultrasonic waves and said electromagnetic waves comprise radio signals or infrared light (see figs 2, 3 elements 202, 302).

9. As to claim 10, Tang teaches the apparatus according to claim 1, wherein said processor is selected from the group consisting of a microprocessor, a micro-controller or other processor, a digital signal processor, and instructions stored in said memory circuit for configuring said programmable logic circuit as a processor (see fig. 8 elements 801, 805 and col. 3 line 63 to col. 4 line 11).

10. As to claim 11, Tang teaches the apparatus according to claim 10, wherein said instructions configure said programmable logic device as a device selected from the group consisting of a microprocessor, a micro-controller, and a digital processor (see col. 3 line 63 to col. 4 line 11).

11. As to claim 12, Tang teaches the apparatus according to claim 1, wherein memory circuit comprised one or more non-volatile memory elements (see fig. 8 element 807).

12. As to claim 13, Tang teaches the apparatus according to claim 1, wherein said programmable logic device comprises one or more memory elements (see fig. 8 element 807).

13. As to claim 14, Tang teaches the apparatus according to claim 13, wherein said memory elements are non-volatile (see fig. 8 element 807).

14. As to claim 15, Tang teaches a method for programming a programmable logic device using a wireless link (see fig 5 elements 402, 502) comprising the step of:

(A) presenting programming signals to a wireless transceiver (see fig. 5 col. 4 lines 18-24); and

(B) programming a programmable logic circuit in response to said program signals, wherein said programmable logic circuit comprised a memory circuit, and a processor in a single integrated circuit package (see fig. 8 elements 800, 803, 806-807, 801 and col. 3 line 63 to col. 4 line 11).

Although the apparatus disclosed by Tang shows substantial features of the claimed invention (discussed above), it fails to explicitly teach: a programmable logic device. Lien; however, teaches said programmable logic circuit comprises a programmable logic device (see fig. 1 elements 20, 22 and col. 3 lines 29-45). Given the teaching of Lien, a person having ordinary skill in the art would have readily recognized the desirability and advantages of modifying Tang by employing the well-known or conventional feature of the apparatus, such as taught by Lien, in order to provide integrating multiple components into a single integrated circuit package.

15. As to claim 17, Tang teaches the method according to claim 15, further comprising the steps of:

(C) during a first bootup, configuring said programmable logic device as said processor in response to instructions stored in said memory circuit (see col. 3 line 63 to col. 4 line 11); and

(D) reprogramming said memory circuit in response to said programming signals (see col. 3 line 63 to col. 4 line 11).

16. As to claim 18, Tang teaches an apparatus (see fig. 8) comprising:

a programmable logic device (see fig. 5 elements 405, 404);

a memory circuit (see fig. 8 element 807);

a processor (see fig. 8 element 801); and

a wireless transceiver (see fig. 5 element 501), wherein said memory circuit, and processor are encased in a single integrated circuit (IC) package (see fig. 8 and col. 3 line 63 to col. 4 line 11).

Although the apparatus disclosed by Tang shows substantial features of the claimed invention (discussed above), it fails to explicitly teach: said programmable logic device is encased in a single integrated circuit (IC) package. Lien; however, teaches said programmable logic device is encased in a single integrated circuit (IC) package (see fig. 1 elements 20, 22 and col. 3 lines 29-45). Given the teaching of Lien, a person having ordinary skill in the art would have readily recognized the desirability and advantages of modifying Tang by employing the well-known or conventional feature of the apparatus, such as taught by Lien, in order to provide integrating multiple components into a single integrated circuit package.

17. As to claim 20, Tang teaches the apparatus according to claim 18, further comprising a transducer coupled to said wireless transceiver (see fig. 5 element "ANTENNA").

18. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tang and Lien in view of Deming et al. (U.S. Pat. No. 5,864,486).

As to claim 3, the combination of Tang and Lien fail to explicitly teach a JEDEC standard integrated circuit package. Deming; however, teaches the integrated circuit comprises a JEDEC standard integrated circuit package (see column 1 lines 27-45). It would have been

obviously a person having ordinary skill in the art to have the JEDEC standard integrated circuit package taught by Deming in order to cover the standardization of discrete semiconductor device (see col. 1 lines 14-23).

19. Claims 4, 16 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tang and Lien in view of Rostoker et al. (U.S. Pat. No. 5,625,563).

As to claims 4, 16 and 19, the combination of Tang and Lien fail to explicitly teach said wireless transceiver is contained within said integrated circuit package. Rostoker; however, teaches said wireless transceiver is contained within said integrated circuit package (see figs 7, 8 and col. 8 line 65 to col. 9 line 42). Given the teaching of Rostoker, a person having ordinary skill in the art would have readily recognized the desirability and advantages of modifying the combination of Tang and Lien by employing the well known or conventional feature of the apparatus, the method and the apparatus, such as taught by Rostoker, in order to provide simple and inexpensive integrated circuit assemblies (see col. 2 lines 54-58).

20. Claims 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tang and Lien in view of Philip S. Esnouf (U.S. Pat. No 5,364,108).

As to claims 7-8, the combination of Tang and Lien fail to explicitly teach: a light emitting/sensitive device, and an ultrasonic transducer; and said light emitting/sensitive device comprises an infrared diode or other type or wavelength of light emitting/sensitive diode or transistor. Esnouf; however, teaches the apparatus wherein said wireless transceiver communicates through a device selected from the group consisting of a light emitting/sensitive device and an ultrasonic transducer (see figure 7 and column 11 lines 12-17 and column 13 lines 43-50); and said light emitting/sensitive device comprises an infrared diode or other type or

wavelength of light emitting/sensitive diode or transistor (see figure 7 and column 11 lines 12-17). Given the teaching of Esnouf, a person having ordinary skill in the art would have readily recognized the desirability and advantages of modifying the combination of Tang and Lien by employing the well known or conventional feature of the apparatus, such as taught by Esnouf, in order to provide transforming signals.

21. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tang and Lien in view of Wang et al. (U.S. Pat. No. 6,448,820).

As to claim 9, the combination of Tang and Lien fail to explicitly teach said processor and said programmable logic device are implemented on a single die. Wang; however, teaches said processor and said programmable logic device are implemented on a single die (see fig. 1 elements 101, 121 and col. 3 lines 15-19). Given the teaching of Wang, a person having ordinary skill in the art would have readily recognized the desirability and advantages of modifying the combination of Tang and Lien by employing the well-known or conventional feature of the apparatus, such as taught by Wang, in order to provide implementing the processor and the PLD into a single integrated die.

Allowable Subject Matter

22. Claim 23 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

23. In response to the applicant's arguments that Tang fails to teach a programmable logic device nor does Lien remedy this deficiency, nor these references would be combinable.

Examiner disagrees, in fig. 1 elements 20, 22 col. 3 lines 29-45 clearly indicates a system on a system on a chip (SOC) 20 having a FPGA (or programmable logic device) and other components such as microprocessor, memory, etc on the chip 20. Therefore, the combination of Tang and Lien teach each and every element of the presently claimed invention.

24. In response to the applicant's argument that Tang fails to teach a programmable logic device. In col. 4 lines 38-62 Tang indicates ISP devices 404 and 405 (a programmable logic device) but he does not disclose the ISP devices integrated on a single circuit package. However, Lien remedy this deficiency by teaching a chip 20 which includes a FPGA, microprocessor, memory, etc. Therefore, Tang teaches configuring the programmable logic device.

25. Applicant argues Lien is silent regarding "interfaces" but this limitation is construed to be new matter (see 35 U.S.C. 112, first paragraph rejection above).

Conclusion

26. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

27. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mike Nguyen whose telephone number is 703 305-5040. The examiner can normally be reached on 8:00AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey Gaffin can be reached on 703 308-3301. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

28. We will move to new site in October so any inquiry concerning this communication or earlier communications after October should be directed to the examiner whose telephone number is 571 272-4153. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey Gaffin can be reached on 571 272-4146.

Mike Nguyen
Patent Examiner
Group Art Unit 2182

JEFFREY GAFFIN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

09/02/2004